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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/020,447	12/18/2001	Thomas D. Fletcher	2207/11269	1709
23838	7590	12/15/2004	EXAMINER	
KENYON & KENYON 1500 K STREET, N.W., SUITE 700 WASHINGTON, DC 20005			MAI, TAN V	
			ART UNIT	PAPER NUMBER
			2124	

DATE MAILED: 12/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/020,447

Applicant(s)

FLETCHER, THOMAS D.

Examiner

Tan V Mai

Art Unit

2124

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 8/31/04, 11/18/02 & 2/28/02.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-42 is/are pending in the application.
- 4a) Of the above claim(s) 1-9 and 26-31 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 10-14, 17-19, 22-25, 32-35, 37, 40 and 41 is/are rejected.
- 7) ☒ Claim(s) 15, 16, 20, 21, 36, 38, 39 and 42 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>11/18/02, 2/28/02</u> . | 6) <input type="checkbox"/> Other: _____ |

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1. Applicant's election of Group II, claims 10-25 and 32-42, in Paper No. filed 8/31/2004 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).
2. The drawings are objected to because the label "Block **210**" (Fig. 2) should be -- Block **120**--. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.
3. Claims 12 and 33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 12, the phrase "determining an **intermediate XOR value** for each of said propagate values and based on the propagate value and corresponding generate value" (line 2) is misdescriptive because the **intermediate value** is either NAND gate (e.g., see element 305 of Fig. 3) or AND gate (e.g., see elements 305 & 308 of Fig. 3) result. The phrase "wherein **intermediate XOR values** are determined without using an XOR gate" is NOT understood. According to Fig. 3, the output of element 308 is **A XOR B** value. The value is XOR value of "two bit addends A & B ". It is NOT the "**intermediate XOR value** for each of said propagate values and based on the

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propagate value and corresponding generate value" as claimed. Clarification is requested. Similarly noted claim 33.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 10, 13, 17 and 19 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Ware (US Pat. 4,623,982).

As per independent claim 10, Ware teaches, e.g., see Figs. 3-4, the claimed invention: including receiving two multibit addends A & B; determining a propagate value K(i) and corresponding generate value G(i); determining a carry-out value (e.g., the combination logic of K(i) & G(i)); and determining a sum value D(i). It is noted that Ware does specifically detail the claimed "one of the carry generation blocks determine exactly three of the carry-output values".

As per dependent claim 13, the claim adds "wherein there is a single critical path through the plurality of carry generation blocks" feature. A parallel adder circuit should have at least one critical path through the plurality of carry generation blocks as claimed.

Due to the similarity of apparatus claims 17 and 19 to claims 10 and 13, they are rejected under a similar rationale.

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6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 10, 12-14, 17, 19, 22-25, 32, 34-35, 37 and 40-41 rejected under 35 U.S.C. 103(a) as being unpatentable over Levin et al.

As per independent claim 10, Levin et al disclose, e.g., see Figs. 5A-5B, the invention substantially as claimed, including: receiving two multibit, i.e., FOUR-bit, addends A & B; determining a propagate value Pi and corresponding generate value Gi, e.g., see Equations (1a)-(1b); determining a carry-out value (e.g., the combination logic of Pi & Gi, see Equation (1c)); and determining a sum value Si. It is noted that Levin et al do NOT specifically detail the claimed "one of the carry generation blocks determine exactly three of the carry-output values"; however, the size of block is obvious design choice for the logic designer, e.g., Persoon et al (US Pat. 5,117,386) or Ware (US Pat. 4,623,982), disclose parallel adders having THREE-bit adder(s). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to design the claimed invention according to Levin et al's teachings because the device is a carry look-ahead adder as claimed.

As per dependent claim 12, the claim adds "determining an intermediate XOR" feature. The examiner believes the feature refer to NAND-INVERT (305, 308). Levin et al do show the equivalent function, e.g., Equation (1c).

As per dependent claim 13, the claim adds "wherein there is a single critical path through the plurality of carry generation blocks" feature. A parallel adder circuit should have at least one critical path through the plurality of carry generation blocks.

As per dependent claim 14, the claim adds "wherein gate in the critical path have tapered transistor stacks" feature. The examiner believes that the "**tapered transistor stacks**" feature is old and well known in the art. For example, a simple and/or combination logic gate could be implemented by such feature, e.g., a two-input CMOS AND gate can be implemented by "**tapered transistor stacks**". Also see Gonfaus et al (Figs. 2-4).

Due to the similarity of apparatus claims 17, 19 and 23 to claims 10 and 12-14, they are rejected under a similar rationale.

As per dependent claim 22, the claim adds "wherein inputs and outputs of gates on the critical path are buffered to reduce the load on the critical path". The feature is obvious to a logic designer to use the buffer [for supplying more current] to reduce the load.

As per dependent claim 24, the claim adds "one or more buffers" feature. The feature is obvious to a logic designer to use the buffer to delay the desired signal(s) of the least significant bit(s) of each block to provide all the outputs at the same time.

As per dependent claim 25, the claim adds "a size that is a multiple of three" is obvious design choice.

As per independent claim 32, Levin et al disclose, e.g., see Figs. 5A-5B, the invention substantially as claimed, including: receiving two multibit addends A & B;

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determining a propagate value P_i and corresponding generate value G_i , e.g., see Equations (1a)-(1b); determining a carry-out value (e.g., the combination logic of P_i & G_i , see Equation 1c); and determining a sum value S_i . It is noted that Levin et al do NOT specifically detail the claimed "carry generation blocks that include a plurality of **tapered transistor stacks**" feature; however, "**tapered transistor stacks**" is broad term [by definition]. A simple and/or combination logic gate could be implemented by such feature, e.g., a two-input CMOS AND gate can be implemented by "**tapered transistor stacks**". It would have been obvious to a person having ordinary skill in the art at the time the invention was made to design the claimed invention according to Levin et al's teachings because the device is a carry look-ahead adder as claimed.

Due to the similarity of claim 34 to claim 13, it is rejected under a similar rationale.

Due to the similarity of claim 35 to claim 14, it is rejected under a similar rationale.

Due to the similarity of independent claim 37 to claim 13, it is rejected under a similar rationale.

Due to the similarity of claim 40 to claim 22, it is rejected under a similar rationale.

Due to the similarity of claim 41 to claim 14, it is rejected under a similar rationale.

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8. Claims 14, 22-25, 32, 34-35, 37 and 40-41 rejected under 35 U.S.C. 103(a) as being unpatentable over Ware (US Pat. 4,623,982).

Ware has been discussed in paragraph #5 above.

As per dependent claim 14, the claim adds "wherein gate in the critical path have tapered transistor stacks" feature. The examiner believes that the "**tapered transistor stacks**" feature is old and well known in the art. For example, a simple and/or combination logic gate could be implemented by such feature, e.g., a two-input CMOS AND gate can be implemented by "**tapered transistor stacks**". Also see Gonfaus et al (Figs. 2-4). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to design the claimed invention according to Ware's teachings because the device is a carry look-ahead adder as claimed.

As per dependent claim 22, the claim adds "wherein inputs and outputs of gates on the critical path are buffered to reduce the load on the critical path". The feature is obvious to a logic designer to use the buffer [for supplying more current] to reduce the load.

Due to the similarity of claim 23 to claim 14, it is rejected under a similar rationale.

As per dependent claim 24, the claim adds "one or more buffers" feature. The feature is obvious to a logic designer to use the buffer to delay the desired signal(s) of the least significant bit(s) of each block to provide all the outputs at the same time.

As per dependent claim 25, the claim adds "a size that is a multiple of three" is obvious design choice.

Due to the similarity of claim 32 to claim 14, it is rejected under a similar rationale.

Due to the similarity of claim 34 to claim 13, it is rejected under a similar rationale.

Due to the similarity of claim 35 to claim 14, it is rejected under a similar rationale.

Due to the similarity of independent claim 37 to claim 13, it is rejected under a similar rationale.

Due to the similarity of claim 40 to claim 22, it is rejected under a similar rationale.

Due to the similarity of claim 41 to claim 14, it is rejected under a similar rationale.

9. Claims 11 and 18 rejected under 35 U.S.C. 103(a) as being unpatentable over Levin et al in view of Vo et al (US Pat. 4,737,92).

Levin et al have been discussed in paragraph #7 above.

As per dependent claim 11, the claim adds "wherein another of the carry generation blocks determines exactly six of the carry-output values. The variable sizes of blocks are obvious design choice for the logic designer, e.g., Vo et al disclose, e.g., see Fig. 5, a plurality of variable block adders, i.e., the sizes are two to six bit and Ware disclose, e.g., see Figs. 3-4, a plurality of variable block adders, i.e., the sizes are two to four bit. It would have been obvious to a person having ordinary skill in the art at the

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time the invention was made to combine Vo et al in Levin et al, thereby making the claimed invention, because the proposed device is a carry look-ahead adder having different block sizes as claimed.

Due to the similarity of claim 18 to claim 11, it is rejected under a similar rationale.

10. Claims 11 and 18 rejected under 35 U.S.C. 103(a) as being unpatentable over Ware in view of Vo et al (US Pat. 4,737,92).

Ware has been discussed in paragraph #8 above.

As per dependent claim 11, the claim adds "wherein another of the carry generation blocks determines exactly six of the carry-output values. The variable sizes of blocks are obvious design choice for the logic designer, e.g., Vo et al disclose, e.g., see Fig. 5, a plurality of variable block adders, i.e., the sizes are two to six bit and Ware disclose, e.g., see Figs. 3-4, a plurality of variable block adders, i.e., the sizes are two to four bit. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine Vo et al in Ware, thereby making the claimed invention, because the proposed device is a carry look-ahead adder having different block sizes as claimed.

Due to the similarity of claim 18 to claim 11, it is rejected under a similar rationale.

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11. Claims 15-16, 20-21, 33, 36, 38-39 and 42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 33 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Cited references are art of interest.

13. The following is an examiner's statement of reasons for allowance: the recorded references do NOT teach or suggest the method / adder having the detail features as recited in dependent claims 15-16, 20-21, 33, 36, 38-39 and 42.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan V. Mai whose telephone number is (571) 272-3726. The examiner can normally be reached on Tue-Fri from 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki, can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is:

Official (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.



TAN V. MAI
PRIMARY EXAMINER